MANIPAL
ACADEMY *of* HIGHER EDUCATION
(Institution of Eminence Deemed to be University)

Master of Engineering - ME (VLSI Design)

Syllabus

July 2022 Onwards

MANIPAL SCHOOL OF INFORMATION SCIENCES
MANIPAL ACADEMY OF HIGHER EDUCATION
MANIPAL – 576104.KARNATAKA. INDIA.

Program Structure

Semester-1	Semester-2
High Level Digital Design	Advanced VLSI Design
Data Structures	Low Power VLSI Design
Digital Systems & VLSI Design	Scripting for VLSI
Verification	Universal Verification Methodology
Elective – I	Elective – II
Mini Project - I	Mini Project - II
Professional Skill Development - I	Professional Skill Development - II
Semester 3 and 4	
Project Work	

Elective -1 Course Name	Elective-2 Course Name
CAD for VLSI	Advanced Logic Synthesis
System on Chip Design	Formal Methods
Digital Signal Processing	Machine Learning for VLSI Design
	Physical Design
	Wireless Communications and Antenna Design
	Entrepreneurship
	IT Project Management
	System Software

SEMESTER I

VLS 5001: High Level Digital Design

Introduction to Digital System and VLSI design Flow; Combinational & Sequential circuits design; logic optimization techniques; finite state machines and optimization; Timing Analysis; FPGA design flow; Digital Design Application: FIFO Design; AMBA Bus Specification – AHB, APB

VLS 5101: Data Structures

Algorithm specification and analysis techniques; Elementary data structures; Sorting & Searching algorithms; Hash Tables, Graphs and Graph searching

VLS 5102: Digital Systems & VLSI Design

MOS transistor theory; CMOS circuit and layout design; Circuit characterization; transistor sizing and scaling, Power dissipation; CMOS Subsystem Design; CMOS Technologies; Layout Design Rules; Manufacturing Issues

VLS 5103: Verification

Introduction to verification and Methodology; Types of Verifications & Approaches; Verification Planning; Assertions; Test bench Infrastructure; Stimulus and Response; Coverage-Driven Verification; Assertions for Formal Tools; System-Level Verification; Processor Integration Verification; Post-Silicon SoC Validation

ELECTIVES - SEMESTER I

VLS 5131: CAD for VLSI

Introduction to VLSI Design Methodologies; Review of VLSI Design Automation Tools; High Level Synthesis and Synthesis Algorithms; Floor Planning and Placement; Routing; Layout Compaction; Review of VLSI Design Automation Tools; High Level Synthesis and Synthesis Algorithms; Floor Planning and Placement; routing; Layout Compaction

VLS 5132: System on Chip Design

Introduction to System Approach, Hardware-Software Codesign; Electronic System Level Flow; Design Principles in SOC Architecture; Processor Selection for SOC, Processor Architecture, RISC Pipeline; Memory Design; Hardware Interconnects; Hardware/Software Interfaces; Application Studies

ESD 5001: Digital Signal Processing

Review: Classification of signals and systems, z-transform, Fourier transform, DFT, convolution, DFT; FFT Algorithms; Filter Structures; Design of FIR filters, IIR Filters; Multirate Signal Processing; Adaptive Filters; DSP Processor

MPT 5100: Mini Project - I

Problem identification, literature survey, formation of detailed specifications.
Design and implementation of the proposed system architecture.
Demonstrate an ability to present and defend project work carried out to a panel of experts.

PSD 5100: Professional Skill Development - I

Topic selection for the presentation, Report writing, slide preparation, presentation to audience

SEMESTER II

VLS 5201: Advanced VLSI Design

CMOS passive elements; Analog MOSFET Models; Current Sources and Sinks; References; CMOS Single Stage Amplifiers; Differential Amplifiers; Frequency Response of Amplifiers; Noise; Operational Amplifiers; Nonlinear Analog Circuits; Dynamic Analog Circuits; Data Converter Fundamentals and Architectures

VLS 5202: Low Power VLSI Design

Introduction to Low Power Design; Overview of power dissipation in CMOS; Circuit techniques for leakage power reduction; Technology scaling for dynamic power reduction, Voltage scaling approaches; Glitch power Reduction techniques; Clock gating; Adiabatic techniques for low power; Logic optimization for low-power; System level issues in multi-voltage designs, Level shifters; Low power design of building blocks

VLS 5203: Scripting for VLSI

Introduction to OS, h/w, kernel, File system, Process; Networking, Version control Variables, Arithmetic, echo, Quotes, Redirection, pipe, filters, Wild cards, exit status, Command line arguments, constructs, cut, paste, tr, uniq, Sed, Grep, Awk and Make command line, Pattern matching, Subroutines, Formats, References, Packages, Modules, Threads, overloading

VLS 5204: Universal Verification Methodology

Overview of UVM; Concepts of Object-Oriented Programming; UVM library basics; Interface UVCs; Automating UVC Creation; Component Configuration and Factory; UVM Callback; Simple Testbench integration; Stimulus generation topics; Register Abstraction Layer; System UVCs and Testbench Integration; TLM Communications

ELECTIVES - SEMESTER II

VLS 5231: Advanced Logic Synthesis

Introduction to logic synthesis; Two-level logic synthesis; Sequential logic synthesis; Multilevel logic synthesis; Technology mapping

VLS 5232: Formal Methods

The relevance of formal methods in hardware and software design: Formal verification of systems – types, Different approaches to formal methods, Specification and verification of reactive systems, Model checking real-time systems.

Theoretical foundations of formal methods: First-order logic, Temporal logic, Transition systems, Timed automaton for real-time specification, Specification of system properties, safety properties, progress properties: fairness and starvation, partial correctness and total correctness

Contemporary technologies for formal verification: NuSMV 2 for hardware verification, Spin for concurrent reactive system verification, UPPAAL for real-time systems

VLS 5233: Machine Learning for VLSI Design

Introduction to machine learning; Linear and Logistic Regression; Instance based learning; Bayesian learning; Logistic Regression; Neural network; Computational learning; Clustering; Machine Learning in VLSI Design; Machine Learning for Lithographic Process Models; Machine Learning Hardware

VLS 5234: Physical Design

CMOS circuit and layout design; Floorplan; Placement; Clock tree synthesis; Routing; RC extraction; Back annotation; Testing

VLS 5235: Wireless Communications and Antenna Design

Introduction to wireless communication; Modern wireless technologies; Wireless and Cellular Communication; Wireless personal area networks; Ad-hoc wireless networks; Antenna design

ENP 5230: Entrepreneurship

Introduction to Entrepreneurship; Entrepreneurial Traits; Process of Entrepreneurship; Business Start-up Process; Business Plan writing; Case studies

ESD 5232: IT Project Management

Software Project Planning; Estimation; Project Schedules; Reviews; Software Requirements; Design and Programming; Software Testing; Understanding Change; Management and Leadership; Managing an Outsourced Project; Process Improvement

ESD 5236: System Software

Assemblers; Loaders and linkers; Compilers; Context Free Grammars; Bottom-up Parsing with LR(k) parsers; Intermediate Code; Introduction to code optimization.

MPT 5200 Mini project - II

Problem identification, literature survey, formation of detailed specifications.
Design and implementation of the proposed system architecture.
Demonstrate an ability to present and defend project work carried out to a panel of experts.

PSD 5200: Professional Skill Development - II

Peer interviews, mock interviews.
Logical reasoning, mathematical aptitude, domain specific problem-solving skills.
Conduction of domain specific knowledge test.

SEMESTERS III & IV

VLS 6098: Project Work

Problem identification, literature survey, formation of detailed requirement specification document.
Design and implementation of the proposed modules with specific test cases.
Detailed report of the work carried out, present, and defend the project work carried out to a panel of experts.